Remarks

In the Final Office Action dated June 4, 2009, the following rejections are presented: claims 1-12 stand rejected under 35 U.S.C. § 102(b) over Flora (U.S. Patent Pub. 5,343,417); and claims 8 and 15 stand rejected under 35 U.S.C. § 112(2). Claims 13-14 and 16-19 are noted as being allowed. Applicant traverses each these rejections per the following discussion which does not acquiesce in any regard to averments in this Office Action (unless Applicant expressly indicates otherwise).

The Office Action was made final with new grounds for rejecting the claims under § 102(b) over the '417 reference and under § 112(2), but without any substantive amendments being previously presented. Moreover, as discussed below, the finality of the Office Action was made without clear intent to address Applicant's arguments which were previously presented in traversing the underlying rejections. As such, Applicant would respectfully request, should any of the rejections be maintained, that the finality of the Office Action be withdrawn.

Regarding the maintained rejection of claims 8 and 15 under 35 U.S.C. § 112(2), Applicant had previously explained that the rejection should be removed because the language in claims 8 and 15 is as required in § 112(2) with support being provided through discussion of various embodiments discussed in connection with and as an alternative to Figures 8, 9 and 10. As the Examiner did not attempt to discuss such rejections under § 112(2) relative to such embodiments, Applicant assumes that the Examiner has improperly construed these claims as though "circuit" refers only to the conventional type of adder in the Wallace tree 40 of Figure 4 of Applicant's specification. To the extent that the Examiner has another position in this regard, Applicant would request that the finality of the instant Office Action be withdrawn and that such position be articulated for consideration by Applicant as would be required under M.P.E.P. 707.07(f). Notwithstanding this traversal, Applicant has offered a slight amendment to claim 8. Should this amendment be entered, there would be no need to address this rejection further.

Applicant respectfully maintains that the § 102(b) rejection should be withdrawn because the cited Flora '417 reference lacks correspondence. The response provided in the instant Office Action merely states that "Applicant's remarks relative to element 21

and the serial adder are not pertinent." Further, with the instant Office Action, again no attempt has been made to present a *prima facie* case of correspondence for any of the dependent claims. Accordingly, Applicant's previously-presented arguments have not been at all addressed as required in M.P.E.P. § 707.07(f).

In view of the above, Applicant would again ask that Applicant's previously-presented arguments be considered and addressed as such effort is expected to render all the claims allowable over the art of record. Should the Examiner disagree, the record would be ripe for appeal at which time the Board would demand a response to Applicant's arguments and such further effort to explain the rejections would result either in the claims being allowable or new grounds being applied.

Regarding the rejection of claims 1-12 under 35 U.S.C. § 102 in view of the '417 reference, Applicant submits that correspondence is lacking and that the rejection should be removed. The '417 reference makes no mention whatsoever of circuits, as claimed by Applicant, for summing addends from multi-bit words and/or any logic circuitry for processing bits from multi-bit words. Rather, the '417 reference explicitly explains that it uses full (8-bit) and half (4-bit) adders for the "primary object of ... increasing multiplier operating speed while providing a minimum chip area." See '417 reference at Col. 1:19-22. Moreover, after discussing the exemplary embodiments, the '417 reference goes on to explain that the particularly taught implementation involves a full-adder versus half-adder approach with deficiencies towards its purpose due to the manner in which the full adder is used. See '417 reference at Col. 4, lines 51 *et seq.* In an effort to address these deficiencies and achieve the above-noted purpose, the '417 reference teaches that a final level (level 4) includes a pair of adders (serial adder 20 and carry look-ahead adder 21) arranged such that the specific length of serial adder 20 permits for faster processing by carry look-ahead adder 21 and less circuit-board real estate to implement adder 21. See '417 reference at Col. 5-37-51, Col. 1:37-41. Accordingly, the rejection should be removed because the '417 reference is directed to a specific type of implementation that neither corresponds to the claimed invention nor even applies to the type of environment (multi-bit words) set forth as part of the claimed invention. Applicant submits that the teachings of the '417 reference are so specific in this regard, the skilled artisan would be led away from any suggestion of attempting to use such teachings in a manner as asserted

in the Office Action. See the cited '417 reference generally and also Col. 5:18-22, and M.P.E.P. § 2143.01.

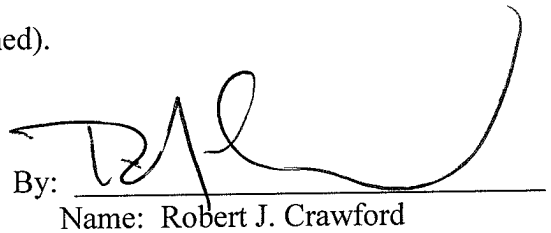
In further support hereof, Applicant would encourage the Examiner to carefully review the '417 reference in further detail to confirm the above-presented characterization and to confirm that the '417 reference makes no mention whatsoever of multi-bit words or a first level for receiving addends of multi-bit words as claimed. For example, at Col. 5:12-27, the '417 reference discusses its adder 21 as having a bit-length that is defined in a manner unrelated to multi-bit words. Long-standing ordinary/dictionary definitions clearly differentiate such commonly-used technical terms, "bits", "bytes" and "words"; see Applicant's specification (*e.g.*, third and fourth paragraphs), the cited '417 reference (*e.g.*, Col. 2:40-51).

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Aaron Waxler, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: 

Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.608PA)